ABSTRACT

A method to test the erase condition of memory cells in a memory array device is achieved. The method is further extended to methods to detect and correct under erase and over erase conditions. The erase condition of a section of the memory array device is altered to form an erased section and non-erased sections. The control gates of the memory cells in the non-erased sections are forced to a normal off-state voltage sufficient to turn off erased cells. The control gates of the memory cells in non-selected subsections of the erased section are forced to a guaranteed off-state voltage that will turn off erased cells including those that are over erased. The control gates of the memory cells in a selected subsection of the erased section are forced to a check voltage. Thereafter, the bitline current of the selected subsection of the erased section is measured to determine erase condition of the selected subsection of the erase section.